REMARKS

INTRODUCTION:

In accordance with the foregoing, claim 18 has been amended. No new matter is being presented, and approval and entry are respectfully requested.

Claims 4-6, 14, and 16-21 are pending and under consideration. Reconsideration is respectfully requested.

REJECTION UNDER 35 U.S.C. §102:

In the Office Action, at pages 2-4, claims 18-21 were rejected under 35 U.S.C. §102(b) as being anticipated by Kitano et al. (USPN 5,608,265; hereafter, Kitano). This rejection is traversed and reconsideration is requested.

Claim 18 has been amended to clarify that the semiconductor device of the present claimed invention is a single multichip package wherein the electronic package carries a number of chips and interconnects them through several layers of conductive patterns, each separated by a layer of insulation and interconnected via holes (see definition of Multichip Package (MCP) in EPPIC Faraday Partnership electronic glossary located at http:/www.eppic-faraday.com/glossary.html, a copy of which is provided herewith for the Examiner's convenience). The multichip package of the present claimed invention is not separable into individual packages for each chip, but rather, is a construct of cooperating elements in a single multichip package.

In contrast, Kitano recites a semiconductor chip, a lead and a member for electrically connecting them together (see Abstract, Kitano). Kitano also recites a plurality of chip packages (see FIG. 10, Kitano; col. 8, lines 10-18):

> A semiconductor apparatus according to a sixth embodiment of the present invention is shown in a cross-sectional view of FIG. 10. In this embodiment, four semiconductor devices as shown in the first embodiment are placed one upon another and the respective leads 4 are connected by way of bumps 5. By constructing the packages in this manner and mounting the lowest package 14-d upon a printed circuit board, the mounting density is increased to be quadrupled. (emphasis added)

By stacking a plurality of separable semiconductor packages, Kitano achieves a multi-pin package, as is illustrated in FIGs. 6, 7, and 17 and col. 6, lines 31-34 of Kitano.

Thus, it is respectfully submitted that the arrangement of Kitano and amended claim 18 of the present invention are structurally different. Hence, amended claim 18 is submitted not to be anticipated under 35 U.S.C. §102(b) by Kitano et al. (USPN 5,608,265). Since claims 19-21 depend from amended claim 18, claims 19-21 are submitted not to be anticipated under

35 U.S.C. §102(b) by Kitano et al. (USPN 5,608,265) for at least the reasons that amended claim 18 is submitted not to be anticipated under 35 U.S.C. §102(b) by Kitano et al. (USPN 5,608,265).

REJECTION UNDER 35 U.S.C. §103:

In the Office Action, at page 4, claims 4-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Kitano et al. (USPN 5,608265; hereafter, Kitano) in view of Itabashi et al. (USPN 6,300,244; hereafter, Itabashi). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

Claim 18 has been amended to show more clearly that the semiconductor package of claim 18 is a semiconductor device multichip package. Since claims 4-6 depend from amended claim 18, claims 4-6 incorporate the features of amended claim 18 and are submitted to be patentable under 35 U.S.C. §103(a) over Kitano et al. (USPN 5,608265) for at least the reasons cited above.

In addition, with respect to claims 5-6, as noted by the Examiner, Kitano does not explicitly disclose that each semiconductor element is electrically connected by flip-chip mounting to a respective wiring pattern and wherein each semiconductor element is electrically connected via an anisotropically conductive film to a respective wiring pattern. Although Itabashi recites a flip-chip mounting, Itabashi also incorporates an inorganic compound and a high melting point metal on the inner surfaces of at least one of the via-hole and the trench (see claims 1 and 10), which is not recited by amended claim 18 of the present invention (from which claims 5-6 depend). Thus, Itabashi teaches away from the present invention, and it is not appropriate to combine Itabashi with Kitano. Hence, claims 4-6 are submitted to be patentable under 35 U.S.C. §103(a) over Itabashi et al. (USPN 6,300,244).

Since it is submitted that it is inappropriate to combine Itabashi with Kitano, it is respectfully submitted that amended claim 18 is patentable under 35 U.S.C. §103(a) over Kitano et al. (USPN 5,608265) in view of Itabashi et al. (USPN 6,300,244). Since claims 4-6 depend from amended claim 18, claims 4-6 are submitted to be patentable under 35 U.S.C. §103(a) over Kitano et al. (USPN 5,608265) in view of Itabashi et al. (USPN 6,300,244) for at least the reasons that amended claim 18 is submitted to be patentable under 35 U.S.C. §103(a) over Kitano et al. (USPN 5,608265) in view of Itabashi et al. (USPN 6,300,244).

ALLOWABLE SUBJECT MATTER:

Claims 14, 16 and 17 were allowed.

Applicant thanks the Examiner for his careful review of the claims and allowance of claims 14, 16 and 17.

EXAMINER'S RESPONSE TO APPLICANT'S AMENDMENT AND ARGUMENTS:

Applicant has reviewed Lauder et al (USPN 6,130,823; hereafter, Lauder) and asserts that Lauder does not anticipate amended independent claim 18 for the reasons previously recited and also based on the amendment to claim 18.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Electronics glossary

Accelerated Stress Test
A test conducted at a stress, e.g., chemical or physical, higher than that encountered in normal operation, for the purpose of producing a measurable effect, such as a fatigue failure, in a shorter time than experienced at operating stresses.

Accelerator
An organic compound which is added to an epoxy resin to shorten the cure time.

Active Components
Electronics components, such as transistors, diodes, electron tubes, thyristors, etc which can operate on an applied electrical signal as to change its basic characteristics ie: rectification, amplification, switching, etc.

Alloy
A solid state solution or compound of two or more metals.
(v.) To melt or make an alloy.

Area Array Tab
Tape automated bonding where edge-located pads and additional pads on the inner surface area of a chip are addressed in the bonding scheme.

Array
A group of elements, such as pads or pins, or circuits arranged in rows and columns on one substrate.

Backbonding
Bonding active chips to the substrate using the back of the chip, leaving the face, with its circuitry face up. The opposite of backbonding is face down bonding.

Backside Metallurgy (BSM)
A metallisation pad electrically connected to internal conductors within a multilayered ceramic package, to which pins are brazed.

Ball bond
A wire bond, usually made with gold or copper wire, in which the wire extending below the capillary is melted to form a ball prior to the first bond being made.

Ball Grid Array (BGA)
A package that has its I/Os, made with solder bumps, across the whole of the surface area rather than just the periphery. Therefore, an area array of solder balls joined to a SCM or MCM is used to electrically and physically connect the package to the next level of package, usually a printed circuit board.

Ball Limiting Metallurgy (BLM)
The solder wettable terminal metallurgy, which defines the size and area of a soldered connection, such as C4 and a chip. The BLM limits the flow of the solder ball to the desired area, and provides adhesion and contact to the chip wiring.

Blind via
A via extending from an interior layer to only one surface of a printed board.

Bond length
Dependent on footprint of tool used in wire bonding.

Bond pad
Contact area on the chip or the substrate to which the wire is to be attached in wire bonding.

Bump
A raised metal feature on a die land or tape carrier tape that facilitates inner lead bonding.

Buried via
A via that connects two or more interior layers of a printed circuit board and does not extend to either surface of the printed circuit board.

C4
Controlled collapse chip connection: a technique of solder joint flip chip connection to a substrate where the surface tension forces of the molten solder controls the height of the joint and supports the weight of the chip.

Capillary
A bonding tool used for ball bonding.

Ceramic
Inorganic, nonmetallic material, such as alumina, beryllia, or glass-ceramic, whose final characteristics are produced by subjection to high temperatures. Often used in forming ceramic-substrates for packaging semiconductor chips.

Ceramic Ball Grid Array (CBGA)
A ceramic package using ball grid array technology. See Ball Grid Array.

Chip
The uncased and normally leadless form of an electronic component part, either passive or active, discrete or integrated. Also referred to as a die.

Chip and wire
Assembly technique which uses discrete wires to interconnect backbonding die to lands, lead frames, etc.

Chip carrier
A low-profile, usually square, surface mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package.

Chip-on-Board (COB)
One of the many configurations in which a chip is directly bonded to a circuit board or substrate. These approaches include wirebonding, TAB, or solder interconnections, similar to the C4 structure. In low-end consumer systems, chip-on-board generally refers to wirebonding of chips directly to board bonded and subsequently protected with a glob of resin material. See also Direct Chip Attach.

Chip Scale Package (CSP)
Chip scale package not much greater than the chip itself (typically not greater than 20% larger).

Component
An element of equipment which unto itself does not form a system. Components can be semiconductors, resistors, etc.

Component density
Quantity of components per unit area of printed circuit board.

Conformal coating
An insulating protective covering that conforms to the configuration of the objects coated (typically printed circuit boards, printed board assembly) providing a barrier against environmental conditions.

COTS
Commercial off-the-shelf.

Creep
Time dependent strain occurring under stress.

Delamination
A separation between plies with a material base, between a base material and a conductive foil, or any other planar separation with a printed board.

Dendritic growth
Metallic filaments that grow between conductors in the presence of condensed moisture and an electric bias.

Die
Integrated circuit chip as cut (diced) from finished wafer. See chip.

Dielectric
Material that does not conduct electricity. Generally used for making capacitors, insulating conductors (as in crossover and multilayered circuits) and for encapsulating circuits.

Dielectric Constant (Dk)
The term used to describe a material's ability to store charge when used as a capacitor dielectric. It is the ratio of the charge that would be stored with free space to that stored with the material in question as the dielectric.

Direct Chip Attach
A name applied to any of the chip-to-substrate connections used to eliminate the first level of packaging. See also Chip-on-Board.

Discrete component
A separate part of a printed circuit board assembly that performs a circuit function (transistor, resistor, capacitor, etc).

Dual-in-Line Package (DIP)
A package having two rows of leads extending at right angles from the base and having standard spacing between leads and between rows of leads. DIPs are made of ceramic (Cerdip) and plastic (Pdip).

Elongation factor
Allowed stretch in the wire during wire bonding.

Embedded component
A discrete component that is fabricated as an integral part of a printed board.

Engineering Change (EC)
A change in design. An electrical design change is frequently implanted by cutting out or adding an electrical path to the manufactured hardware, e.g., laser deleting a line or adding a wire on a ceramic substrate.

Flex circuit
A pliable circuit that will bend, usually made of polyester or polyimide.

Flip Chip
Unpackaged silicon dies that have been supplied with solder balls directly on the active side of the die. They are called flip chips because they are flipped upside-down, compared to a conventional wirebonded chip.

Flux
Rosin used in solder operations to remove surface oxides.

FR4
Fire retardant polymer/glass fibre cloth laminate used to make PCBs.

Gull wing
An SMT lead type. The lead extends horizontally from the component body centre, bends down immediately past the body and then bends outwards just below the bottom of the body.

Heel crack
Common fault in wedge bond where the wire has been cracked due to severe bending or from the wire bonding tool.

Hybrid Circuit
An insulating base material with various combinations of interconnected film conductors, film components, semiconductor die, passive components, and bonding wire which form an electronic circuit.

Integrated Circuit (IC)
A miniature or microelectronic device that integrates such elements as transistors, resistors, dielectrics and capacitors into an electrical circuit possessing a specific function. Form the basis of all modern electronic products.

Intellectual Property (IP)
Property produced by effort of the mind, as distinct from real or personal property. Intellectual property may or may not enjoy the benefit of legal protection.

Interconnect
A highly conductive material, usually aluminium or polysilicon, that carries electrical signals to different parts of a die.

ISO
International Standards Organization.

J-lead
A type of surface mount lead. The lead comes out of the package body near the z-axis centreline, is formed down, then rolled under the package in a 'J' shape.

Kirkendall voids
Voids across the interface between 2 different materials, formed in the material having the greater rate of diffusion.

Laminate
Raw material for printed circuits consisting of a plastic sheet with copper foil tracks on one or both sides.

Land
An interconnection site on a PCB.

Lithography
The process in semiconductor manufacturing in which chip designs are projected onto silicon wafers.

Loop height
Bond wire height between the first and second bond in wire bonding.

MEMS
Micro-Electro-Mechanical Systems.

Micro ball grid array
a small ball grid array also known as a chip scale package.

Microelectronics
Those micro devices, such as integrated circuits, which are fabricated in sub-micron dimensions and which form the basis of all electronic products.

Microfocus xray
Real time x-ray.

Microsystems
Microminiaturized and integrated systems based on microelectronics, photonics, RF, micro-electro-mechanical systems (MEMS) and packaging technologies.

Moore's Law
Moore's Law is an observation made in 1965 by Intel co-founder Gordon Moore that the number of transistors on a chip doubles about every 18 months, which translates to higher performance for roughly the same manufacturing cost.

Multilayer Ceramic (MLC)

Ceramic substrate consisting of multiple layers of metals and ceramics interconnected with vias.

Multichip Module (MCM)
Two or more die are attached to the same substrate and wire bonded.

Multichip Package (MCP)
An electronic package that caries a number of chips and interconnects them through several layers of conductive patterns. Each one is separated by a layer of insulation and interconnected via holes.

Nano
One thousand millionth.

Nanotechnology
The development and use of devices that have a size of only less than 200 nanometres.

Optoelectronics
The combination of photonics and microelectronics. When they are packaged together, they provide the capacity to generate, transport and manipulate data at phenomenal rates.

Package
A container for die providing protection and connection to the next level of integration.

Packaging
The bridge that interconnects the ICs and other components into a system-level board to form electronic products.

Passives
Circuit elements such as resistors and capacitors which do not change state when subjected to voltage or current.

Pad/Pin Grid Array (PGA)
PGA may refer to a pad grid array or a pin grid array. A pad grid array refers to a packaging technology in which a device's external connections are arranged as an array of conducting pads on the base of the package. A pin grid array refers to a packaging technology in which a device's external connections are arranged as an array of conducting leads, or pins, on the base of the package.

Photonics
The technology that uses light particles (photons) to carry information over hair-thin fibres of very pure glass.

Plastic package
Environmentally protected chip, embedded in a transfer moulded resin.

Printed Circuit Board (PCB)
A type of circuit board which has conducting tracks superimposed, or 'printed', on one or both sides, and may also contain internal signal layers and power and ground planes. An alternative name, Printed Wire Board (PWB), is commonly used in America.

Radio Frequency (RF)
That part of the spectrum from approximately 50kHz to gigahertz.

Reflow spike
The portion of the reflow soldering process during which the temperature of the solder is raised to a value sufficient to cause the solder to melt.

Screen Printing
Printing through a screen or stencil.

Semiconductor
A special class of materials that can exhibit both conducting and insulating properties.

Silicon
A brittle, grey, crystalline chemical element which, in its pure state, serves as a semiconductor substrate in microelectronics. It is naturally found in compounds such as silicon dioxide.

Single Chip Package (SCP)
A package that supports a single microelectronics device so that its electrical, mechanical, thermal and chemical performance needs are adequately served.

SOC
System-on-a-Chip.

SOP
System-on-Package - A single component, multi-function, multi-chip package providing all the needed system-level functions. Functions include analog, digital, optical, RF and MEMS.

Sonotrode
Horn which couples the ultrasonic energy from the generator to the tool.

Stitch length
Overall length between the first and second wire bond, generally restricted to 100 the wire diameter.

Solder
A low melting point alloy used in numerous joining applications in microelectronics. The most common solders are lead-tin alloys. Typical solder contains 60% tin and 40% lead - increasing the proportion of lead results in a softer solder with a lower melting point, while decreasing the proportion of lead results in a harder solder with a higher melting point.

Stand off height
Height of component above the PCB.

Surface Insulation Resistance
The electrical resistance of an insulation material between a pair of contacts, conductors or grounding devices in various combinations, determined under specified environmental and electrical conditions.

Surface Mount Technology (SMT)
A method of assembling hybrid circuits and printed wiring boards where component parts are mounted onto, rather than into, the printed-wiring boards, as in the mounting components on substrates in hybrid technology.

Tape Automated Bonding (TAB)
The process where silicon chips are joined to patterned metal on polymer tape (e.g., copper on polymide), using thermocompression bonding, and subsequently attached to a substrate or board by outer lead bonding. Intermediate processing may be carried out in strip form through operations such as testing, encapsulation, burn-in, and excising the individual packages from the tape.

Time out of bag
Time a component is exposed to a humid atmosphere.

Underfill
Encapsulant material typically deposited between a flip chip device and substrate to reduce a mismatch in thermal expansion coefficients.

Vias
Interconnects in a multilevel PCB.

Void
A gas entrapment in a solder joint.

Wafers
Slices of semiconductor crystal materials used as substrates for monolithic ICs, diodes and transistors.

Wedge bond
A bond made by a bonding tool or capillary directly pressing against a round wire.

Wire Bonding
The method used to attach very fine wire to semiconductor components to interconnect these components with each other or with package leads.